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Attorney's Docket No. NSC1-G0610
[P04402]

In re Patent Application of:

KAMESH V. GADEPALLY

Application No.: 10/006,334

Filed: December 3, 2001

For: **METHOD FOR MANUFACTURING AN INTEGRATED CIRCUIT STRUCTURE WITH LIMITED SOURCE SALICIDATION**

Group Art Unit: 2818

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is a *Appellant's Brief* (in triplicate) in the above-identified application.

1. __ No additional fee is required.

2. X Check in the amount of $330.00 is enclosed.

3. X Please charge any additional fees, including any fees necessary for extensions of time, or credit overpayment to Deposit Account No. 50-1697. **A duplicate copy of this sheet is enclosed**.

4. __ Petition for extension of time. The undersigned attorney of record hereby petitions for an extension of time pursuant to 37 C.F.R. section 1.136(a), as may be required, to file this response.

CERTIFICATE OF MAILING

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Dated: DECEMBER 5, 2003 By: Marsha A. Townsend
Marsha A. Townsend

GIRARD & EQUITZ LLP

Dated: 12/5/03 By: Alfred A Equitz
Alfred A. Equitz
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Attorney for Applicant(s)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

KAMESH V. GADEPALLY

Application No. 10/006,334

Filed: December 3, 2001

For: **METHOD FOR MANUFACTURING AN INTEGRATED CIRCUIT STRUCTURE WITH LIMITED SOURCE SALICIDATION**

Group Art Unit: 2818

Examiner: QUOC DINH HOANG

APPELLANT'S BRIEF

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GIRARD & EQUITZ LLP Date: 12/05/03

By: Marsha A. Townsend
Marsha A. Townsend

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant commenced this appeal from the final rejection of claims 1-13 in the referenced application by filing a Notice of Appeal on October 21, 2003, from the decision dated September 17, 2003, of the Primary Examiner finally rejecting claims 1-13 of the application. This Brief is filed in triplicate to further Appellant's appeal to the Board of Appeals and Interferences from the final rejection of claims 1-13 of the application.

Real Party in Interest

The real party in interest is National Semiconductor Corporation, to whom the present application has been assigned (as evidenced by the assignment recorded at Reel 012660, Frame 0890, on February 27, 2002).

Related Appeals and Interferences

There are no related appeals or interferences known to appellant, appellant's representative, or the assignee.

Status of the Claims

Claims 1-13 are pending. Claims 1-13 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,087,227 (Hsu) in view of U.S. Patent 6,197,646 (Goto).

Status of Amendments

No amendment has been filed since the final rejection of claims 1-13.

Summary of the Invention

The invention is a method for forming metal salicide regions and metal salicide exclusion regions during integrated circuit (IC) manufacture. When performing the method, a metal layer is deposited in a controlled manner on an IC structure (e.g., a metal layer having a predetermined thickness is deposited on the IC structure). Portions of the metal layer are then removed from locations where the metal salicide exclusion regions are to be formed. Then, the remaining (non-removed) metal undergoes a "source limited" salicidation reaction to form the metal salicide regions. The salicidation reaction is "source limited" in the sense that it is limited by the amount of metal available for reaction, so that the available metal is entirely consumed by the reaction.

The metal available for the source limited salicidation reaction is the metal remaining after deposited metal has been removed from locations where metal salicide exclusion regions are to be formed. Thus, the metal available for the source limited salicidation reaction is limited by the pre-reaction metal-removal step and by the manner in which the metal deposition step is performed, so that the available metal is entirely consumed by the reaction. By controlling the thickness of the deposited metal layer, and removing portions of the deposited metal (before the salicidation reaction) from locations where metal salicide exclusion regions are to be formed, the salicidation reaction can be driven to completion so that the reaction ceases when all available metal has been consumed.

By source-limiting the salicidation reaction, the invention eliminates the need for post-reaction removal of residual (unreacted) metal from the vicinity of the metal salicide regions formed. As explained in the specification at page 9, line 23-page 10, line 8, the

"source limited" nature of the reaction can also significantly reduce metal salicide crawl over and under the desired metal salicide exclusion regions (e.g., over and under gate sidewall spacers 124 adjacent to metal salicide regions 130 shown in Fig. 9 of the application) below the levels attainable using conventional metal salicide forming methods in which the salicidation reaction is not source limited.

Copies of Figs. 4-9 of the application are attached. An embodiment of the method of claim 1 (and claim 13) is described in the specification with reference to Figs. 4-9. This embodiment includes the steps of:

(a) providing the IC structure shown in Fig. 4, which includes MOS transistor structures 104 and 106 having exposed silicon surfaces;

(b) depositing metal layer 126 (shown in Fig. 5) on the IC structure in a controlled manner (so that metal layer 126 has a predetermined thickness, preferably in the range from 150 angstroms to 500 angstroms, as mentioned in the specification at page 8, lines 5-6);

(c) forming photoresist masking layer 128 (shown in Fig. 6) on portions of the MOS transistor structures where metal salicide regions are to be formed;

(d) removing metal layer 126 from those MOS transistor structures (e.g., the Fig. 7 structure including gate sidewall spacers 124, silicon gate 122, and gate oxide layers 110) where metal salicide exclusion regions are to be formed;

(e) after step (d), stripping photoresist masking layer 128 (to convert the Fig. 7 structure to the Fig. 8 structure); and

(f) after step (e), reacting metal in metal layer 126 with silicon (in exposed silicon surfaces of gate 120 and substrate 102) in a source limited manner to form metal salicide regions 130 of Fig. 9,

wherein step (b) includes the step of controlling a metal deposition parameter such that metal layer 126 has at least one predetermined property (i.e., thickness) that causes the reaction during step (f) to occur in a source limited manner and limits metal salicide crawl during step (f) beyond structures where metal salicide regions 130 are to be formed.

The specification teaches (at page 7, line 29-page 8, line 5) that metal layer 126 can be a cobalt layer, and that a capping layer (e.g., a titanium or titanium nitride capping layer) can be deposited on the cobalt layer (as recited in claim 8). In embodiments in which a

cobalt layer and a capping layer are deposited, the metal salicide regions formed in accordance with the invention are cobalt salicide regions (as recited in claim 8).

The specification teaches (at page 9, line 23-page 10, line 8) that the invention can be performed in a manner that significantly limits metal salicide crawl over and under at least one portion of an MOS structure where metal salicide regions are to be formed (as recited in claims 5 and 12).

The specification teaches (at page 7, line 32-page 8, line 2) that the deposited metal layer can comprise metal selected from the group consisting of cobalt, titanium, tantalum, nickel and molybdenum as recited in claim 6, and teaches (at page 8, lines 5-6) that the deposited metal layer can have a thickness in the range of 150 to 500 angstroms as recited in claim 7.

Issues

1. Are claims 1-13 patentable over Hsu?
2. Are claims 1-13 patentable over Goto?
3. Are claims 1-13 patentable over Hsu in view of Goto?

Grouping of the Claims

For purposes of this appeal, each dependent claim stands or falls with the independent claim from which it depends.

Arguments

1. Claims 1-13 are patentable over Hsu.

The Examiner has cited Hsu's teaching with reference to Figs. 1-3 of Hsu (we refer to Hsu's Figs. 1A-1D collectively as Fig. 1, to Hsu's Figs. 2A-2G collectively as Fig. 2, and to Hsu's Figs. 3A-3F collectively as Fig. 3). However, Hsu does not teach how the salicide regions of Fig. 1 (e.g., salicide layers 234 and 236 shown in Fig. 1A) are formed.

The method disclosed in Hsu for forming the salicide regions of Hsu's Fig. 3 is identical to the method disclosed in Hsu for forming the salicide regions of Hsu's Fig. 2 insofar as Hsu's teaching is relevant to the claims on appeal. This method includes the steps of depositing a metal layer (layer 330 of Fig. 2 or layer 430 of Fig. 3), removing portions of the metal layer (the portions removed to convert the Fig. 2C structure to the Fig. 2D structure, or the portions removed to convert the Fig. 3C structure to the Fig. 3D structure), and then reacting metal in the remaining portions of the metal layer to form metal salicide regions (salicide 350 of Fig. 2G or salicide 430 of Fig. 3F).

Hsu teaches at col. 5, lines 39-50, that after a salicidation reaction is performed on metal 330 of Fig. 2F, unreacted metal 330 (an "unreaction portion of the metal layer 330") is removed to leave salicide regions 350 exposed (as shown in Fig. 2G). Similarly, Hsu teaches at col. 6, line 65-col. 7, line 5, that after a salicidation reaction is performed on metal 430 of the Fig. 3E structure, unreacted metal 430 (an "unreaction portion of the metal layer 430") is removed ("by, for example, dry etching") to leave salicide regions 450 exposed (as shown in Fig. 3F). Thus, the metal salicide forming method taught by Hsu with reference to Hsu's Figs. 2 and 3 does not include the step of performing a "source limited" salicidation reaction, as recited in each finally rejected independent claim. Rather, Hsu teaches away from the invention by teaching a metal salicide region-forming method that including the step of performing a salicidation reaction that is not source limited, so that post-reaction removal of unreacted metal is required.

Hsu fails to teach or suggest a method including the steps of depositing metal layer 330 or 430 (or any other metal layer), removing the metal layer from MOS transistor structures where metal salicide exclusion regions are to be formed, and then reacting remaining portions of the metal layer with silicon of MOS transistor structures to form metal salicide regions, in which a metal deposition parameter is controlled such that the metal layer has a predetermined property causing the reaction to occur in a source limited manner and limiting metal (e.g., cobalt) salicide crawl during formation of the metal salicide regions (as recited in claims 1 and 8). Nor does Hsu teach or suggest a method including the steps of depositing a metal layer having a predetermined thickness over an IC structure, removing the metal layer from MOS transistor structures where metal salicide exclusion regions are to be

formed, and then reacting remaining portions of the metal layer with silicon of the MOS transistor structures to form metal salicide regions in a source limited manner (as recited in claim 13).

Rather than teaching or suggesting the claimed invention, Hsu teaches away from the invention by teaching a method in which more metal (330 or 430) is deposited (and allowed to remain available for reaction) than is consumed during a subsequent salicide-forming reaction. For example, Hsu teaches at col. 6, line 65-col. 7, line 5, that unreacted metal 430 should be removed (e.g., by dry etching) from over the underlying structure after a salicide-forming reaction, to leave salicide layers 450 exposed (as shown in Fig. 3F). Hsu's salicide layers 450 are not formed in a source limited manner since, after Hsu's salicidation reaction, unreacted metal remains over the underlying structures. This unreacted metal must be removed to leave salicide layers 450 exposed.

2. Claims 1-13 are patentable over Goto.

Goto also fails to teach formation of metal salicide regions in a source limited manner as recited in claims 1, 8, and 13.

The Examiner cites Goto's Fig. 6A (and the description thereof at Goto's cols. 10-11) and Fig. 7A (which is described at Goto's col. 6) in support of the contention that Goto teaches control of a cobalt deposition parameter such that a deposited cobalt layer has a predetermined property such that a cobalt salicide layer (formed by subsequent reaction of the cobalt) has a predetermined attribute (e.g., sheet resistance).

The Examiner also contends at page 5 of the final Office Action that although Goto does not "expressly disclose reducing salicide crawl, clearly in Figure 7A, no salicide crawl is formed beyond the portions of the MOS transistor structure where metal salicide regions are to be formed."

However, Goto fails to teach or suggest a source limited metal salicide-forming reaction as recited in claims 1, 8, and 13, and Goto instead teaches away from the claimed

invention by teaching removal of residual (unreacted) metal from the vicinity of Goto's metal salicide regions after a salicidation reaction (with reference to Goto's Figs. 1E and 1F).

Goto's teaching (at col. 10, line 50 – col. 11, line 8) with reference to Fig. 6A (and at col. 10, lines 45-49) does not amount to a teaching or suggestion to perform a source limited metal salicide-forming reaction as recited in claims 1, 8, and 13. Rather Goto's teaching with reference to Fig. 6A is merely a general teaching that control of the thickness of a deposited metal layer affects the sheet resistance of metal salicide formed by a subsequent silicidation reaction and post-reaction annealing. For example, Goto teaches at col. 10, line 59 to col. 11, line 4, that a sufficiently thick metal layer (thicker than 5 nm) should be used to achieve a desirably low metal salicide sheet resistance, since use of a thinner metal layer (thinner than 5 nm) would result in a higher metal salicide sheet resistance. Goto also teaches at col. 10, lines 45-49, that deposition of a metal layer that is too thick (i.e., a metal layer having thickness greater than 15 nm, where gate length is 0.3 μm or less) can (during subsequent salicidation of the metal) result in "destruction" of semiconductor junctions that are intended to underlie metal salicide to be formed during the salicidation reaction, but this clearly does not amount to a teaching to control deposited metal thickness to cause subsequent salicidation of the metal to occur in a source limited manner. Goto's teaching at col. 10, line 45- col. 11, line 8, cannot reasonably be construed as a teaching or suggestion to perform a salicidation reaction in a source limited manner. On the other hand, Goto's teaching (with reference to Figs. 1D, 1E, 1F, and 7A) to perform post-salicide-forming reaction removal of residual (unreacted) metal amounts to a teaching (away from the invention) to perform a salicidation reaction in a non-source-limited manner rather than a source limited manner, as discussed below.

Goto teaches depositing metal (e.g., cobalt layer 11 of Goto's Fig. 1D), and titanium nitride (TiN layer 12 of Goto's Fig. 1D) over the metal, over all regions of a semiconductor structure. A silicidation reaction is then performed before any of metal 11 is removed from over any portion of the structure where a salicide exclusion region is to be formed (in contrast with the method of claim 1, 8, or 13). Goto teaches at col. 9, lines 5-12, that the reaction forms metal salicide (e.g., salicide 11g, 11d, and 11s of Fig. 1E) under the overlying titanium nitride layer, as shown in Fig. 1E. Then, as described at col. 9, lines 13-20, titanium nitride 12 is removed and unreacted (residual) metal 11 is then removed to produce a structure with

exposed metal salicide 11d, 11s, and 11g (the structure shown in Fig. 1F). Because unreacted metal 11 is removed after the reaction, the reaction is not source limited. After the reaction, an annealing operation is performed to lower the resistance of the metal salicide. If Goto's silicidation reaction were source limited, Goto would not need to remove residual (unreacted) metal 11 from the vicinity of Goto's metal salicide regions after Goto's salicidation reaction. However, Goto's silicidation reaction is not source limited because Goto teaches post-reaction removal of residual metal with reference to Figs. 1E and 1F.

To form the structure shown in Goto's Fig. 7A, Goto teaches (at col. 6) performance of operations similar to those described in Goto with reference Figs. 1D, 1E, and 1F. A continuous layer of metal (e.g., titanium or cobalt) is deposited over all regions of a semiconductor structure. A silicidation reaction (including two annealing stages) is then performed before any of the metal is removed from over any portion of the structure where a salicide exclusion region is to be formed (in contrast with the method of claim 1, 8, or 13). Then, as described at col. 6, lines 46-47, unreacted metal is removed to produce the Fig. 7A structure which has exposed metal silicide 58. Goto's teaching with reference to Fig. 7A does not amount to a teaching or suggestion to perform a source limited metal salicide-forming reaction as recited in claims 1, 8, and 13.

Goto also fails to teach formation of metal salicide regions in a manner that limits metal (e.g. cobalt) salicide crawl, as recited in claims 1 and 8. The Examiner acknowledges that Goto "does not disclose reducing salicide crawl." However, the Examiner argues that the structure of Goto's Fig. 7A exhibits "no salicide crawl ... beyond the portions of the MOS transistor structure where metal salicide regions are to be formed." Appellant respectfully contends that the lack of clearly apparent salicide crawl in Fig. 7A in no way implies that no such salicide crawl would result from implementing Goto's explicit teachings. There is no teaching or suggestion determinable from Goto that Fig. 7A is drawn to scale and is not a simplified drawing. The present application teaches that a conventional method such as Goto's (in which a silicidation reaction is not source limited) would result in salicide crawl, and that such salicide crawl could be significantly reduced if the inventive method (in which the salicide-forming reaction is source limited) were performed rather than the conventional method. Goto teaches that there is excess metal available during Goto's silicidation reaction,

that the unreacted (excess) metal is removed after the reaction, and that there is no metal removal (before Goto's silicidation reaction) from over structures which are to be metal salicide exclusion regions. There is no teaching or suggestion determinable from Goto that Goto's method would prevent, and no reason to believe that Goto's method would inherently prevent, salicide crawl beyond the portions of a MOS transistor structure where metal salicide regions are to be formed.

Goto fails to teach or suggest a method including the steps of depositing a metal layer, then removing the metal layer from MOS transistor structures where metal salicide exclusion regions are to be formed, and then reacting remaining portions of the metal layer with silicon of MOS transistor structures to form metal salicide regions, in which a metal deposition parameter is controlled such that the metal layer has a predetermined property causing the reaction to occur in a source limited manner and limiting metal (e.g., cobalt) salicide crawl during formation of the metal salicide regions (as recited in claims 1 and 8). Nor does Goto teach or suggest a method including the steps of depositing a metal layer having a predetermined thickness over an IC structure, removing the metal layer from MOS transistor structures where metal salicide exclusion regions are to be formed, and then reacting remaining portions of the metal layer with silicon of the MOS transistor structures to form metal salicide regions in a source limited manner (as recited in claim 13).

Rather than teaching or suggesting a source limited salicidation reaction as recited in claims 1, 8, and 13, Goto teaches away from the claimed invention by teaching (e.g., at col. 9, lines 13-20) with reference to Figs. 1D, 1E, and 1F a conventional method in which more metal (11) is deposited, and allowed to remain available for reaction, than is consumed during a subsequent salicide-forming reaction. Goto also teaches away from the invention by teaching (e.g., at col. 6, lines 46-47) with reference to Fig. 7A a conventional method in which more metal is deposited, and allowed to remain available for reaction, than is consumed during a subsequent salicide-forming reaction.

As noted above, Goto also fails to teach formation of metal salicide regions in a manner that limits metal (e.g. cobalt) salicide crawl as recited in claims 1 and 8.

3. Claims 1-13 are patentable over Hsu in view of Goto.

As explained above, each of claims 1, 8, and 13 is patentable over Hsu considered alone and over Goto considered alone. The Examiner contends that it would have been obvious to modify Hsu's teaching by depositing a "predetermined thickness" of metal during Hsu's pre-reaction metal deposition step in accordance with Goto's teaching to reach the invention of claims 1, 8, and 13. Appellant contends that because both Hsu and Goto teach away from the claimed invention, each of claims 1, 8, and 13 is patentable over Hsu and Goto, considered alone or in combination. Appellant also contends that modification of Hsu's method in accordance with the teaching of Goto would not eliminate Hsu's step of post-salicidation reaction removal of unreacted metal (so that the modified Hsu method would not include performance of a salicidation reaction in a source limited manner), since both Goto and Hsu teach formation of metal salicide regions by a method including the steps of non-source-limited salicidation followed by post-reaction removal of unreacted metal.

Goto's teaching (at col. 10, line 50 – col. 11, line 8) to control of the thickness of a deposited metal layer is merely a teaching to control such thickness for the purpose of achieving a desired sheet resistance of metal salicide formed by subsequent salicidation reaction of the metal (followed by annealing). Goto teaches in this context (at col. 10, line 59-col. 11, line 4) that a sufficiently thick metal layer (thicker than 5 nm) should be used to achieve a desirably low metal salicide sheet resistance, since use of a thinner metal layer (thinner than 5 nm) would result in a higher metal salicide sheet resistance. This teaching of Goto cannot reasonably be construed as a teaching to modify Hsu's method to deposit a sufficiently thin layer of metal to limit the amount of metal available for Hsu's salicidation reaction so that the so-modified salicidation reaction is performed in a source limited manner (i.e., so that all metal present during the reaction is consumed and so that no post-reaction excess metal removal is required). Goto's teaching does not amount to a teaching or suggestion to modify Hsu's method to achieve a source limited salicidation reaction as recited in claims 1, 8, and 13.

Rather than teaching or suggesting modification of Hsu's method to achieve a source limited salicidation reaction as recited in claims 1, 8, and 13, Goto teaches away from the claimed invention by teaching (e.g., at col. 9, lines 13-20) with reference to Figs. 1D, 1E, and

1F a method in which more metal (11) is deposited (and allowed to remain available for reaction) than is consumed during a subsequent salicide-forming reaction, and by teaching (e.g., at col. 6, lines 46-47) with reference to Fig. 7A a method in which more metal is deposited (and allowed to remain available for reaction) than is consumed during a subsequent salicide-forming reaction, as well as by teaching deposition of a sufficiently thick metal layer to achieve desirably low metal salicide sheet resistance (in contrast with a sufficiently thin metal layer to ensure consumption of all metal in a subsequent salicide-forming reaction). In view of this teaching away from the claimed invention, it cannot reasonably be contended that Goto's disclosure would have suggested to one of ordinary skill in the art that Hsu's method should be modified to perform Hsu's salicidation reaction in a source limited manner. Rather, modification of Hsu's method in accordance with Goto's teaching would result in deposition of a sufficiently thick metal layer (on the structure disclosed in Hsu) to achieve desirably low sheet resistance of the metal salicide resulting from the modified Hsu method, without elimination of the step of post-reaction removal of unreacted metal (and thus without performing the salicidation reaction of the modified Hsu method in a source limited manner).

Nor does Goto's teaching (at col. 6, lines 41-47) that during formation of Goto's Fig. 7A structure, a "predetermined thickness" of metal is deposited during a pre-reaction metal deposition step, amount to a teaching nor a suggestion to control deposited metal thickness so as to achieve a source limited reaction (in which all metal present at the start of the reaction reacts) as claimed. However, this is not a teaching to control deposited metal thickness so as to achieve a source limited reaction (in which all metal present at the start of the reaction reacts), and does not amount to a teaching or suggestion to modify Hsu's method to reach the invention of claim 1, 8, or 13. Rather, at col. 6, lines 46-47, Goto teaches away from the invention by teaching that the Fig. 7A structure should be formed by a method in which more metal is deposited (and allowed to remain available for reaction) than is consumed during a subsequent salicide-forming reaction, and that the unreacted excess metal should be removed (after the reaction). It cannot reasonably be contended that Goto's teaching at col. 6, lines 41-47, amounts to a teaching or suggestion to modify Hsu's method to achieve a source limited salicidation reaction as recited in claims 1, 8, and 13. Modification of Hsu's method in accordance with the teaching of Goto would not eliminate Hsu's step of post-salicidation

reaction removal of unreacted metal, since both Goto and Hsu teach formation of metal salicide regions by a method including the step of post-salicidation reaction removal of unreacted metal.

Appellant contends that there is no teaching determinable from Goto that Hsu's method should be modified to reach the invention of claim 1, 8, or 13. Absent such teaching determinable from Goto or other specifically identified art of record, it is improper to reject claims 1, 8, and 13 on the basis of an unsupported assertion that it would have been obvious to modify Hsu's method to reach the claimed invention. For the foregoing reasons, Appellant contends that claims 1, 8, and 13 (and all claims depending therefrom) are patentable over Hsu and Goto, whether these references are considered individually or in combination.

Respectfully submitted,
GIRARD & EQUITZ LLP

Dated: 12/5/03 By: Alfred A Equitz

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Reg. No. 30,922

Attorneys for Appellant

Attorney Docket No. NSC1-G0610 [P04402 P01]

CLAIMS ON APPEAL

1. (twice amended) A method for forming metal salicide regions and metal salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

(a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

(b) depositing a metal layer on the IC structure in a controlled manner;

(c) forming a photoresist masking layer on portions of the MOS transistor structures where metal salicide regions are to be formed;

(d) removing the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed;

(e) after step (d), stripping the photoresist masking layer; and

(f) after step (e), reacting metal in the metal layer with silicon in the exposed silicon surfaces to form metal salicide regions, wherein

step (b) includes the step of controlling at least one metal deposition parameter such that the metal layer has at least one predetermined property that causes the reaction of the metal with the silicon during step (f) to occur in a source limited manner and limits metal salicide crawl during step (f) beyond at least one of the portions of the MOS transistor structures where metal salicide regions are to be formed.

2. (amended) The method of claim 1, wherein said at least one predetermined property is such that at least one of the metal salicide regions has a predetermined sheet resistance.

3. (amended) The method of claim 1, wherein said at least one predetermined property is such that at least one of the metal salicide regions has a predetermined conductivity.

4. (original) The method of claim 1, where said at least one predetermined property of the metal layer is a thickness of said metal layer.

5. (Amended) The method of claim 1, wherein the removal during step (d) of the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed, and step (b), are performed in a manner significantly limiting metal salicide crawl during step (f) over and under at least one of the portions of the MOS structures where metal salicide regions are to be formed.

6. (original) The method of claim 1, wherein the metal layer deposited in step (b) comprises metal selected from the group consisting of cobalt, titanium, tantalum, nickel and molybdenum.

7. (original) The method of claim 1 wherein the metal layer deposited in step (b) has a thickness in the range of 150 to 500 angstroms.

8. (Twice amended) A method for forming cobalt salicide regions and cobalt salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

(a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

(b) depositing a cobalt layer on the IC structure in a controlled manner;

(c) depositing a capping layer on the cobalt layer;

(d) forming a photoresist masking layer on portions of the MOS transistor structures where cobalt salicide regions are to be formed;

(e) removing the capping layer and the cobalt layer from those MOS transistor structures where cobalt salicide exclusion regions are to be formed;

(f) after step (e), stripping the photoresist masking layer; and

(g) after step (f), reacting cobalt in the cobalt layer with silicon in the exposed silicon surfaces to form cobalt salicide regions, wherein

step (b) includes the step of controlling at least one metal deposition parameter such that the cobalt layer has at least one predetermined property that causes the reaction of the cobalt with the silicon during step (g) to occur in a source limited manner and limits cobalt salicide crawl during step (g) beyond at least one of the portions of the MOS transistor structures where cobalt salicide regions are to be formed.

9. (amended) The method of claim 8, wherein said at least one predetermined property is such that at least one of the cobalt salicide regions has a predetermined sheet resistance.

10. (amended) The method of claim 8, wherein said at least one predetermined property is such that at least one of the cobalt salicide regions has a predetermined conductivity.

11. (original) The method of claim 8, where said at least one predetermined property of the cobalt layer is a thickness of said cobalt layer.

12. (amended) The method of claim 8, wherein the removal during step (e) of the cobalt layer from those MOS transistor structures where cobalt salicide exclusion regions are to be formed, and step (b), are performed in a manner significantly limiting cobalt salicide crawl during step (g) over and under at least one of the portions of the MOS structures where cobalt salicide regions are to be formed.

13. A method for forming metal salicide regions and metal salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

then, depositing a metal layer having a predetermined thickness over the IC structure;

then, forming a photoresist masking layer on those MOS transistor structures where metal salicide regions are to be formed;

then, removing the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed;

then, stripping of the photoresist masking layer from those MOS transistor structures where metal salicide regions are to be formed; and

then, reacting remaining portions of the metal layer with silicon of the MOS transistor structures to form metal salicide regions in a source limited manner.

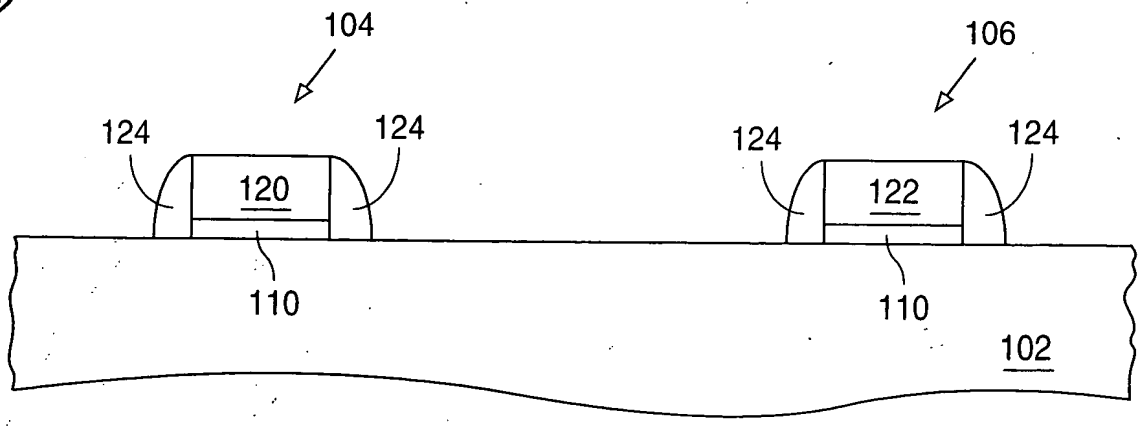

FIG. 4

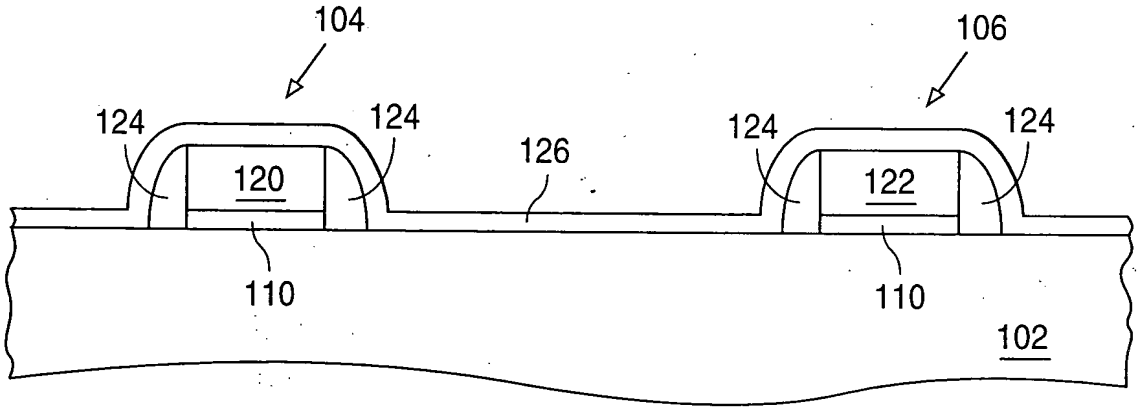

FIG. 5

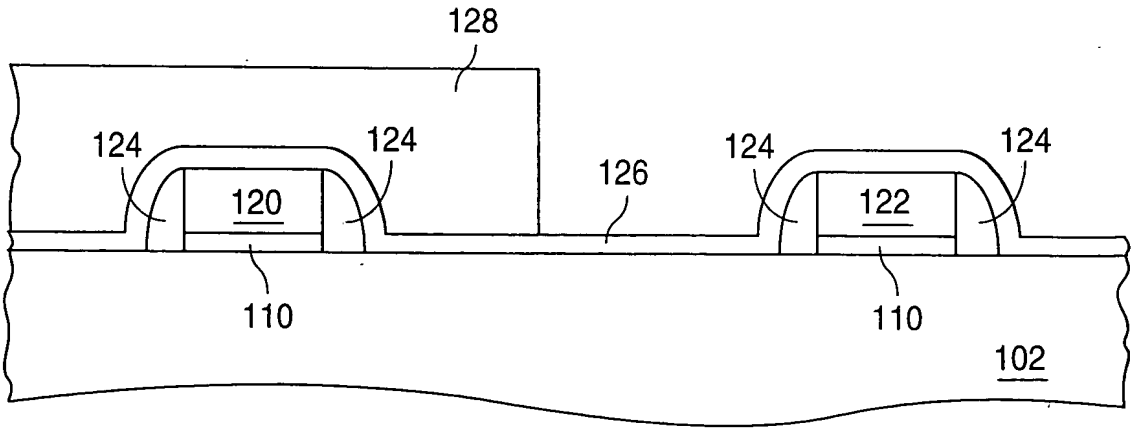

FIG. 6

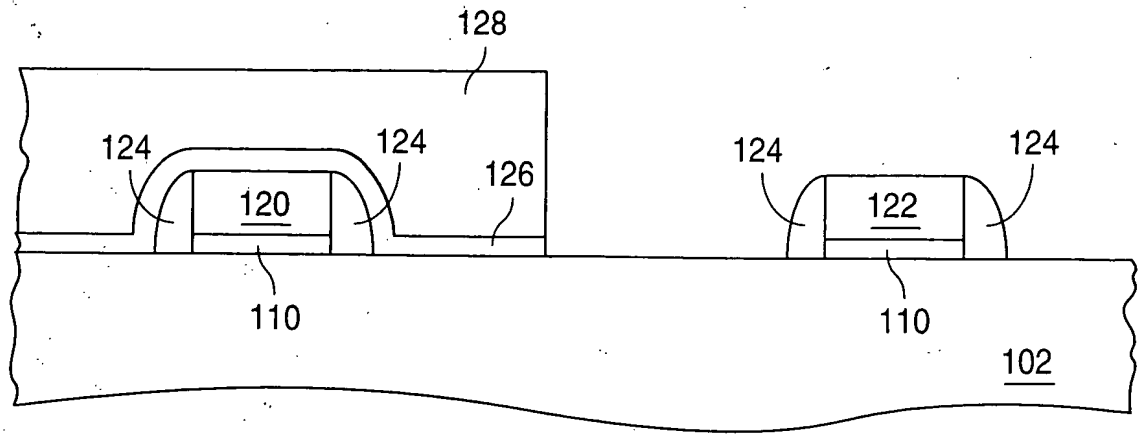

FIG. 7

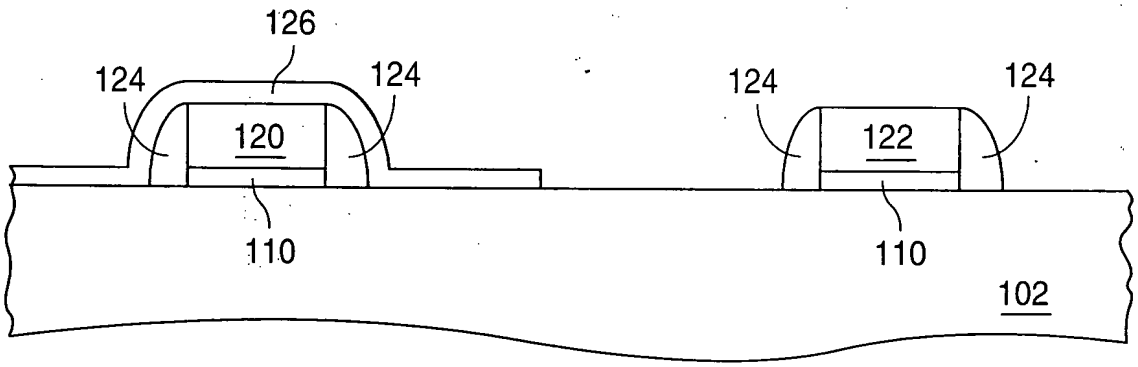

FIG. 8

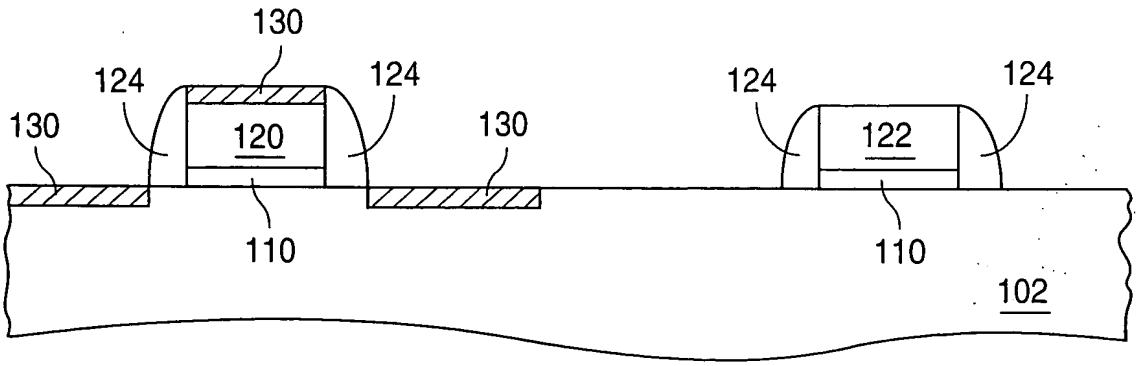

FIG. 9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

KAMESH V. GADEPALLY

Application No. 10/006,334

Filed: December 3, 2001

For: **METHOD FOR MANUFACTURING AN INTEGRATED CIRCUIT STRUCTURE WITH LIMITED SOURCE SALICIDATION**

Group Art Unit: 2818

Examiner: QUOC DINH HOANG

APPELLANT'S BRIEF

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CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on December 5, 2003.

GIRARD & EQUITZ LLP Date: 12/05/03

By: Marsha A. Townsend
Marsha A. Townsend

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant commenced this appeal from the final rejection of claims 1-13 in the referenced application by filing a Notice of Appeal on October 21, 2003, from the decision dated September 17, 2003, of the Primary Examiner finally rejecting claims 1-13 of the application. This Brief is filed in triplicate to further Appellant's appeal to the Board of Appeals and Interferences from the final rejection of claims 1-13 of the application.

Real Party in Interest

The real party in interest is National Semiconductor Corporation, to whom the present application has been assigned (as evidenced by the assignment recorded at Reel 012660, Frame 0890, on February 27, 2002).

Related Appeals and Interferences

There are no related appeals or interferences known to appellant, appellant's representative, or the assignee.

Status of the Claims

Claims 1-13 are pending. Claims 1-13 stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,087,227 (Hsu) in view of U.S. Patent 6,197,646 (Goto).

Status of Amendments

No amendment has been filed since the final rejection of claims 1-13.

Summary of the Invention

The invention is a method for forming metal salicide regions and metal salicide exclusion regions during integrated circuit (IC) manufacture. When performing the method, a metal layer is deposited in a controlled manner on an IC structure (e.g., a metal layer having a predetermined thickness is deposited on the IC structure). Portions of the metal layer are then removed from locations where the metal salicide exclusion regions are to be formed. Then, the remaining (non-removed) metal undergoes a "source limited" salicidation reaction to form the metal salicide regions. The salicidation reaction is "source limited" in the sense that it is limited by the amount of metal available for reaction, so that the available metal is entirely consumed by the reaction.

The metal available for the source limited salicidation reaction is the metal remaining after deposited metal has been removed from locations where metal salicide exclusion regions are to be formed. Thus, the metal available for the source limited salicidation reaction is limited by the pre-reaction metal-removal step and by the manner in which the metal deposition step is performed, so that the available metal is entirely consumed by the reaction. By controlling the thickness of the deposited metal layer, and removing portions of the deposited metal (before the salicidation reaction) from locations where metal salicide exclusion regions are to be formed, the salicidation reaction can be driven to completion so that the reaction ceases when all available metal has been consumed.

By source-limiting the salicidation reaction, the invention eliminates the need for post-reaction removal of residual (unreacted) metal from the vicinity of the metal salicide regions formed. As explained in the specification at page 9, line 23-page 10, line 8, the

"source limited" nature of the reaction can also significantly reduce metal salicide crawl over and under the desired metal salicide exclusion regions (e.g., over and under gate sidewall spacers 124 adjacent to metal salicide regions 130 shown in Fig. 9 of the application) below the levels attainable using conventional metal salicide forming methods in which the salicidation reaction is not source limited.

Copies of Figs. 4-9 of the application are attached. An embodiment of the method of claim 1 (and claim 13) is described in the specification with reference to Figs. 4-9. This embodiment includes the steps of:

(a) providing the IC structure shown in Fig. 4, which includes MOS transistor structures 104 and 106 having exposed silicon surfaces;

(b) depositing metal layer 126 (shown in Fig. 5) on the IC structure in a controlled manner (so that metal layer 126 has a predetermined thickness, preferably in the range from 150 angstroms to 500 angstroms, as mentioned in the specification at page 8, lines 5-6);

(c) forming photoresist masking layer 128 (shown in Fig. 6) on portions of the MOS transistor structures where metal salicide regions are to be formed;

(d) removing metal layer 126 from those MOS transistor structures (e.g., the Fig. 7 structure including gate sidewall spacers 124, silicon gate 122, and gate oxide layers 110) where metal salicide exclusion regions are to be formed;

(e) after step (d), stripping photoresist masking layer 128 (to convert the Fig. 7 structure to the Fig. 8 structure); and

(f) after step (e), reacting metal in metal layer 126 with silicon (in exposed silicon surfaces of gate 120 and substrate 102) in a source limited manner to form metal salicide regions 130 of Fig. 9,

wherein step (b) includes the step of controlling a metal deposition parameter such that metal layer 126 has at least one predetermined property (i.e., thickness) that causes the reaction during step (f) to occur in a source limited manner and limits metal salicide crawl during step (f) beyond structures where metal salicide regions 130 are to be formed.

The specification teaches (at page 7, line 29-page 8, line 5) that metal layer 126 can be a cobalt layer, and that a capping layer (e.g., a titanium or titanium nitride capping layer) can be deposited on the cobalt layer (as recited in claim 8). In embodiments in which a

cobalt layer and a capping layer are deposited, the metal salicide regions formed in accordance with the invention are cobalt salicide regions (as recited in claim 8).

The specification teaches (at page 9, line 23-page 10, line 8) that the invention can be performed in a manner that significantly limits metal salicide crawl over and under at least one portion of an MOS structure where metal salicide regions are to be formed (as recited in claims 5 and 12).

The specification teaches (at page 7, line 32-page 8, line 2) that the deposited metal layer can comprise metal selected from the group consisting of cobalt, titanium, tantalum, nickel and molybdenum as recited in claim 6, and teaches (at page 8, lines 5-6) that the deposited metal layer can have a thickness in the range of 150 to 500 angstroms as recited in claim 7.

Issues

1. Are claims 1-13 patentable over Hsu?
2. Are claims 1-13 patentable over Goto?
3. Are claims 1-13 patentable over Hsu in view of Goto?

Grouping of the Claims

For purposes of this appeal, each dependent claim stands or falls with the independent claim from which it depends.

Arguments

1. Claims 1-13 are patentable over Hsu.

The Examiner has cited Hsu's teaching with reference to Figs. 1-3 of Hsu (we refer to Hsu's Figs. 1A-1D collectively as Fig. 1, to Hsu's Figs. 2A-2G collectively as Fig. 2, and to Hsu's Figs. 3A-3F collectively as Fig. 3). However, Hsu does not teach how the salicide regions of Fig. 1 (e.g., salicide layers 234 and 236 shown in Fig. 1A) are formed.

The method disclosed in Hsu for forming the salicide regions of Hsu's Fig. 3 is identical to the method disclosed in Hsu for forming the salicide regions of Hsu's Fig. 2 insofar as Hsu's teaching is relevant to the claims on appeal. This method includes the steps of depositing a metal layer (layer 330 of Fig. 2 or layer 430 of Fig. 3), removing portions of the metal layer (the portions removed to convert the Fig. 2C structure to the Fig. 2D structure, or the portions removed to convert the Fig. 3C structure to the Fig. 3D structure), and then reacting metal in the remaining portions of the metal layer to form metal salicide regions (salicide 350 of Fig. 2G or salicide 430 of Fig. 3F).

Hsu teaches at col. 5, lines 39-50, that after a salicidation reaction is performed on metal 330 of Fig. 2F, unreacted metal 330 (an "unreaction portion of the metal layer 330") is removed to leave salicide regions 350 exposed (as shown in Fig. 2G). Similarly, Hsu teaches at col. 6, line 65-col. 7, line 5, that after a salicidation reaction is performed on metal 430 of the Fig. 3E structure, unreacted metal 430 (an "unreaction portion of the metal layer 430") is removed ("by, for example, dry etching") to leave salicide regions 450 exposed (as shown in Fig. 3F). Thus, the metal salicide forming method taught by Hsu with reference to Hsu's Figs. 2 and 3 does not include the step of performing a "source limited" salicidation reaction, as recited in each finally rejected independent claim. Rather, Hsu teaches away from the invention by teaching a metal salicide region-forming method that including the step of performing a salicidation reaction that is not source limited, so that post-reaction removal of unreacted metal is required.

Hsu fails to teach or suggest a method including the steps of depositing metal layer 330 or 430 (or any other metal layer), removing the metal layer from MOS transistor structures where metal salicide exclusion regions are to be formed, and then reacting remaining portions of the metal layer with silicon of MOS transistor structures to form metal salicide regions, in which a metal deposition parameter is controlled such that the metal layer has a predetermined property causing the reaction to occur in a source limited manner and limiting metal (e.g., cobalt) salicide crawl during formation of the metal salicide regions (as recited in claims 1 and 8). Nor does Hsu teach or suggest a method including the steps of depositing a metal layer having a predetermined thickness over an IC structure, removing the metal layer from MOS transistor structures where metal salicide exclusion regions are to be

formed, and then reacting remaining portions of the metal layer with silicon of the MOS transistor structures to form metal salicide regions in a source limited manner (as recited in claim 13).

Rather than teaching or suggesting the claimed invention, Hsu teaches away from the invention by teaching a method in which more metal (330 or 430) is deposited (and allowed to remain available for reaction) than is consumed during a subsequent salicide-forming reaction. For example, Hsu teaches at col. 6, line 65-col. 7, line 5, that unreacted metal 430 should be removed (e.g., by dry etching) from over the underlying structure after a salicide-forming reaction, to leave salicide layers 450 exposed (as shown in Fig. 3F). Hsu's salicide layers 450 are not formed in a source limited manner since, after Hsu's salicidation reaction, unreacted metal remains over the underlying structures. This unreacted metal must be removed to leave salicide layers 450 exposed.

2. Claims 1-13 are patentable over Goto.

Goto also fails to teach formation of metal salicide regions in a source limited manner as recited in claims 1, 8, and 13.

The Examiner cites Goto's Fig. 6A (and the description thereof at Goto's cols. 10-11) and Fig. 7A (which is described at Goto's col. 6) in support of the contention that Goto teaches control of a cobalt deposition parameter such that a deposited cobalt layer has a predetermined property such that a cobalt salicide layer (formed by subsequent reaction of the cobalt) has a predetermined attribute (e.g., sheet resistance).

The Examiner also contends at page 5 of the final Office Action that although Goto does not "expressly disclose reducing salicide crawl, clearly in Figure 7A, no salicide crawl is formed beyond the portions of the MOS transistor structure where metal salicide regions are to be formed."

However, Goto fails to teach or suggest a source limited metal salicide-forming reaction as recited in claims 1, 8, and 13, and Goto instead teaches away from the claimed

invention by teaching removal of residual (unreacted) metal from the vicinity of Goto's metal salicide regions after a salicidation reaction (with reference to Goto's Figs. 1E and 1F).

Goto's teaching (at col. 10, line 50 – col. 11, line 8) with reference to Fig. 6A (and at col. 10, lines 45-49) does not amount to a teaching or suggestion to perform a source limited metal salicide-forming reaction as recited in claims 1, 8, and 13. Rather Goto's teaching with reference to Fig. 6A is merely a general teaching that control of the thickness of a deposited metal layer affects the sheet resistance of metal salicide formed by a subsequent silicidation reaction and post-reaction annealing. For example, Goto teaches at col. 10, line 59 to col. 11, line 4, that a sufficiently thick metal layer (thicker than 5 nm) should be used to achieve a desirably low metal salicide sheet resistance, since use of a thinner metal layer (thinner than 5 nm) would result in a higher metal salicide sheet resistance. Goto also teaches at col. 10, lines 45-49, that deposition of a metal layer that is too thick (i.e., a metal layer having thickness greater than 15 nm, where gate length is 0.3 μm or less) can (during subsequent salicidation of the metal) result in "destruction" of semiconductor junctions that are intended to underlie metal salicide to be formed during the salicidation reaction, but this clearly does not amount to a teaching to control deposited metal thickness to cause subsequent salicidation of the metal to occur in a source limited manner. Goto's teaching at col. 10, line 45- col. 11, line 8, cannot reasonably be construed as a teaching or suggestion to perform a salicidation reaction in a source limited manner. On the other hand, Goto's teaching (with reference to Figs. 1D, 1E, 1F, and 7A) to perform post-salicide-forming reaction removal of residual (unreacted) metal amounts to a teaching (away from the invention) to perform a salicidation reaction in a non-source-limited manner rather than a source limited manner, as discussed below.

Goto teaches depositing metal (e.g., cobalt layer 11 of Goto's Fig. 1D), and titanium nitride (TiN layer 12 of Goto's Fig. 1D) over the metal, over all regions of a semiconductor structure. A silicidation reaction is then performed before any of metal 11 is removed from over any portion of the structure where a salicide exclusion region is to be formed (in contrast with the method of claim 1, 8, or 13). Goto teaches at col. 9, lines 5-12, that the reaction forms metal salicide (e.g., salicide 11g, 11d, and 11s of Fig. 1E) under the overlying titanium nitride layer, as shown in Fig. 1E. Then, as described at col. 9, lines 13-20, titanium nitride 12 is removed and unreacted (residual) metal 11 is then removed to produce a structure with

exposed metal salicide 11d, 11s, and 11g (the structure shown in Fig. 1F). Because unreacted metal 11 is removed after the reaction, the reaction is not source limited. After the reaction, an annealing operation is performed to lower the resistance of the metal salicide. If Goto's silicidation reaction were source limited, Goto would not need to remove residual (unreacted) metal 11 from the vicinity of Goto's metal salicide regions after Goto's salicidation reaction. However, Goto's silicidation reaction is not source limited because Goto teaches post-reaction removal of residual metal with reference to Figs. 1E and 1F.

To form the structure shown in Goto's Fig. 7A, Goto teaches (at col. 6) performance of operations similar to those described in Goto with reference Figs. 1D, 1E, and 1F. A continuous layer of metal (e.g., titanium or cobalt) is deposited over all regions of a semiconductor structure. A silicidation reaction (including two annealing stages) is then performed before any of the metal is removed from over any portion of the structure where a salicide exclusion region is to be formed (in contrast with the method of claim 1, 8, or 13). Then, as described at col. 6, lines 46-47, unreacted metal is removed to produce the Fig. 7A structure which has exposed metal silicide 58. Goto's teaching with reference to Fig. 7A does not amount to a teaching or suggestion to perform a source limited metal salicide-forming reaction as recited in claims 1, 8, and 13.

Goto also fails to teach formation of metal salicide regions in a manner that limits metal (e.g. cobalt) salicide crawl, as recited in claims 1 and 8. The Examiner acknowledges that Goto "does not disclose reducing salicide crawl." However, the Examiner argues that the structure of Goto's Fig. 7A exhibits "no salicide crawl ... beyond the portions of the MOS transistor structure where metal salicide regions are to be formed." Appellant respectfully contends that the lack of clearly apparent salicide crawl in Fig. 7A in no way implies that no such salicide crawl would result from implementing Goto's explicit teachings. There is no teaching or suggestion determinable from Goto that Fig. 7A is drawn to scale and is not a simplified drawing. The present application teaches that a conventional method such as Goto's (in which a silicidation reaction is not source limited) would result in salicide crawl, and that such salicide crawl could be significantly reduced if the inventive method (in which the salicide-forming reaction is source limited) were performed rather than the conventional method. Goto teaches that there is excess metal available during Goto's silicidation reaction,

that the unreacted (excess) metal is removed after the reaction, and that there is no metal removal (before Goto's silicidation reaction) from over structures which are to be metal salicide exclusion regions. There is no teaching or suggestion determinable from Goto that Goto's method would prevent, and no reason to believe that Goto's method would inherently prevent, salicide crawl beyond the portions of a MOS transistor structure where metal salicide regions are to be formed.

Goto fails to teach or suggest a method including the steps of depositing a metal layer, then removing the metal layer from MOS transistor structures where metal salicide exclusion regions are to be formed, and then reacting remaining portions of the metal layer with silicon of MOS transistor structures to form metal salicide regions, in which a metal deposition parameter is controlled such that the metal layer has a predetermined property causing the reaction to occur in a source limited manner and limiting metal (e.g., cobalt) salicide crawl during formation of the metal salicide regions (as recited in claims 1 and 8). Nor does Goto teach or suggest a method including the steps of depositing a metal layer having a predetermined thickness over an IC structure, removing the metal layer from MOS transistor structures where metal salicide exclusion regions are to be formed, and then reacting remaining portions of the metal layer with silicon of the MOS transistor structures to form metal salicide regions in a source limited manner (as recited in claim 13).

Rather than teaching or suggesting a source limited salicidation reaction as recited in claims 1, 8, and 13, Goto teaches away from the claimed invention by teaching (e.g., at col. 9, lines 13-20) with reference to Figs. 1D, 1E, and 1F a conventional method in which more metal (11) is deposited, and allowed to remain available for reaction, than is consumed during a subsequent salicide-forming reaction. Goto also teaches away from the invention by teaching (e.g., at col. 6, lines 46-47) with reference to Fig. 7A a conventional method in which more metal is deposited, and allowed to remain available for reaction, than is consumed during a subsequent salicide-forming reaction.

As noted above, Goto also fails to teach formation of metal salicide regions in a manner that limits metal (e.g. cobalt) salicide crawl as recited in claims 1 and 8.

3. Claims 1-13 are patentable over Hsu in view of Goto.

As explained above, each of claims 1, 8, and 13 is patentable over Hsu considered alone and over Goto considered alone. The Examiner contends that it would have been obvious to modify Hsu's teaching by depositing a "predetermined thickness" of metal during Hsu's pre-reaction metal deposition step in accordance with Goto's teaching to reach the invention of claims 1, 8, and 13. Appellant contends that because both Hsu and Goto teach away from the claimed invention, each of claims 1, 8, and 13 is patentable over Hsu and Goto, considered alone or in combination. Appellant also contends that modification of Hsu's method in accordance with the teaching of Goto would not eliminate Hsu's step of post-salicidation reaction removal of unreacted metal (so that the modified Hsu method would not include performance of a salicidation reaction in a source limited manner), since both Goto and Hsu teach formation of metal salicide regions by a method including the steps of non-source-limited salicidation followed by post-reaction removal of unreacted metal.

Goto's teaching (at col. 10, line 50 – col. 11, line 8) to control of the thickness of a deposited metal layer is merely a teaching to control such thickness for the purpose of achieving a desired sheet resistance of metal salicide formed by subsequent salicidation reaction of the metal (followed by annealing). Goto teaches in this context (at col. 10, line 59-col. 11, line 4) that a sufficiently thick metal layer (thicker than 5 nm) should be used to achieve a desirably low metal salicide sheet resistance, since use of a thinner metal layer (thinner than 5 nm) would result in a higher metal salicide sheet resistance. This teaching of Goto cannot reasonably be construed as a teaching to modify Hsu's method to deposit a sufficiently thin layer of metal to limit the amount of metal available for Hsu's salicidation reaction so that the so-modified salicidation reaction is performed in a source limited manner (i.e., so that all metal present during the reaction is consumed and so that no post-reaction excess metal removal is required). Goto's teaching does not amount to a teaching or suggestion to modify Hsu's method to achieve a source limited salicidation reaction as recited in claims 1, 8, and 13.

Rather than teaching or suggesting modification of Hsu's method to achieve a source limited salicidation reaction as recited in claims 1, 8, and 13, Goto teaches away from the claimed invention by teaching (e.g., at col. 9, lines 13-20) with reference to Figs. 1D, 1E, and

1F a method in which more metal (11) is deposited (and allowed to remain available for reaction) than is consumed during a subsequent salicide-forming reaction, and by teaching (e.g., at col. 6, lines 46-47) with reference to Fig. 7A a method in which more metal is deposited (and allowed to remain available for reaction) than is consumed during a subsequent salicide-forming reaction, as well as by teaching deposition of a sufficiently thick metal layer to achieve desirably low metal salicide sheet resistance (in contrast with a sufficiently thin metal layer to ensure consumption of all metal in a subsequent salicide-forming reaction). In view of this teaching away from the claimed invention, it cannot reasonably be contended that Goto's disclosure would have suggested to one of ordinary skill in the art that Hsu's method should be modified to perform Hsu's salicidation reaction in a source limited manner. Rather, modification of Hsu's method in accordance with Goto's teaching would result in deposition of a sufficiently thick metal layer (on the structure disclosed in Hsu) to achieve desirably low sheet resistance of the metal salicide resulting from the modified Hsu method, without elimination of the step of post-reaction removal of unreacted metal (and thus without performing the salicidation reaction of the modified Hsu method in a source limited manner).

Nor does Goto's teaching (at col. 6, lines 41-47) that during formation of Goto's Fig. 7A structure, a "predetermined thickness" of metal is deposited during a pre-reaction metal deposition step, amount to a teaching nor a suggestion to control deposited metal thickness so as to achieve a source limited reaction (in which all metal present at the start of the reaction reacts) as claimed. However, this is not a teaching to control deposited metal thickness so as to achieve a source limited reaction (in which all metal present at the start of the reaction reacts), and does not amount to a teaching or suggestion to modify Hsu's method to reach the invention of claim 1, 8, or 13. Rather, at col. 6, lines 46-47, Goto teaches away from the invention by teaching that the Fig. 7A structure should be formed by a method in which more metal is deposited (and allowed to remain available for reaction) than is consumed during a subsequent salicide-forming reaction, and that the unreacted excess metal should be removed (after the reaction). It cannot reasonably be contended that Goto's teaching at col. 6, lines 41-47, amounts to a teaching or suggestion to modify Hsu's method to achieve a source limited salicidation reaction as recited in claims 1, 8, and 13. Modification of Hsu's method in accordance with the teaching of Goto would not eliminate Hsu's step of post-salicidation

reaction removal of unreacted metal, since both Goto and Hsu teach formation of metal salicide regions by a method including the step of post-salicidation reaction removal of unreacted metal.

Appellant contends that there is no teaching determinable from Goto that Hsu's method should be modified to reach the invention of claim 1, 8, or 13. Absent such teaching determinable from Goto or other specifically identified art of record, it is improper to reject claims 1, 8, and 13 on the basis of an unsupported assertion that it would have been obvious to modify Hsu's method to reach the claimed invention. For the foregoing reasons, Appellant contends that claims 1, 8, and 13 (and all claims depending therefrom) are patentable over Hsu and Goto, whether these references are considered individually or in combination.

Respectfully submitted,
GIRARD & EQUITZ LLP

Dated: 12/5/03 By: Alfred A Equitz

Alfred A. Equitz
Reg. No. 30,922

Attorneys for Appellant

Attorney Docket No. NSC1-G0610 [P04402 P01]

CLAIMS ON APPEAL

1. (twice amended) A method for forming metal salicide regions and metal salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

(a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

(b) depositing a metal layer on the IC structure in a controlled manner;

(c) forming a photoresist masking layer on portions of the MOS transistor structures where metal salicide regions are to be formed;

(d) removing the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed;

(e) after step (d), stripping the photoresist masking layer; and

(f) after step (e), reacting metal in the metal layer with silicon in the exposed silicon surfaces to form metal salicide regions, wherein

step (b) includes the step of controlling at least one metal deposition parameter such that the metal layer has at least one predetermined property that causes the reaction of the metal with the silicon during step (f) to occur in a source limited manner and limits metal salicide crawl during step (f) beyond at least one of the portions of the MOS transistor structures where metal salicide regions are to be formed.

2. (amended) The method of claim 1, wherein said at least one predetermined property is such that at least one of the metal salicide regions has a predetermined sheet resistance.

3. (amended) The method of claim 1, wherein said at least one predetermined property is such that at least one of the metal salicide regions has a predetermined conductivity.

4. (original) The method of claim 1, where said at least one predetermined property of the metal layer is a thickness of said metal layer.

5. (Amended) The method of claim 1, wherein the removal during step (d) of the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed, and step (b), are performed in a manner significantly limiting metal salicide crawl during step (f) over and under at least one of the portions of the MOS structures where metal salicide regions are to be formed.

6. (original) The method of claim 1, wherein the metal layer deposited in step (b) comprises metal selected from the group consisting of cobalt, titanium, tantalum, nickel and molybdenum.

7. (original) The method of claim 1 wherein the metal layer deposited in step (b) has a thickness in the range of 150 to 500 angstroms.

8. (Twice amended) A method for forming cobalt salicide regions and cobalt salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

(a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

(b) depositing a cobalt layer on the IC structure in a controlled manner;

(c) depositing a capping layer on the cobalt layer;

(d) forming a photoresist masking layer on portions of the MOS transistor structures where cobalt salicide regions are to be formed;

(e) removing the capping layer and the cobalt layer from those MOS transistor structures where cobalt salicide exclusion regions are to be formed;

(f) after step (e), stripping the photoresist masking layer; and

(g) after step (f), reacting cobalt in the cobalt layer with silicon in the exposed silicon surfaces to form cobalt salicide regions, wherein

step (b) includes the step of controlling at least one metal deposition parameter such that the cobalt layer has at least one predetermined property that causes the reaction of the cobalt with the silicon during step (g) to occur in a source limited manner and limits cobalt salicide crawl during step (g) beyond at least one of the portions of the MOS transistor structures where cobalt salicide regions are to be formed.

9. (amended) The method of claim 8, wherein said at least one predetermined property is such that at least one of the cobalt salicide regions has a predetermined sheet resistance.

10. (amended) The method of claim 8, wherein said at least one predetermined property is such that at least one of the cobalt salicide regions has a predetermined conductivity.

11. (original) The method of claim 8, where said at least one predetermined property of the cobalt layer is a thickness of said cobalt layer.

12. (amended) The method of claim 8, wherein the removal during step (e) of the cobalt layer from those MOS transistor structures where cobalt salicide exclusion regions are to be formed, and step (b), are performed in a manner significantly limiting cobalt salicide crawl during step (g) over and under at least one of the portions of the MOS structures where cobalt salicide regions are to be formed.

13. A method for forming metal salicide regions and metal salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of:

providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces;

then, depositing a metal layer having a predetermined thickness over the IC structure;

then, forming a photoresist masking layer on those MOS transistor structures where metal salicide regions are to be formed;

then, removing the metal layer from those MOS transistor structures where metal salicide exclusion regions are to be formed;

then, stripping of the photoresist masking layer from those MOS transistor structures where metal salicide regions are to be formed; and

then, reacting remaining portions of the metal layer with silicon of the MOS transistor structures to form metal salicide regions in a source limited manner.

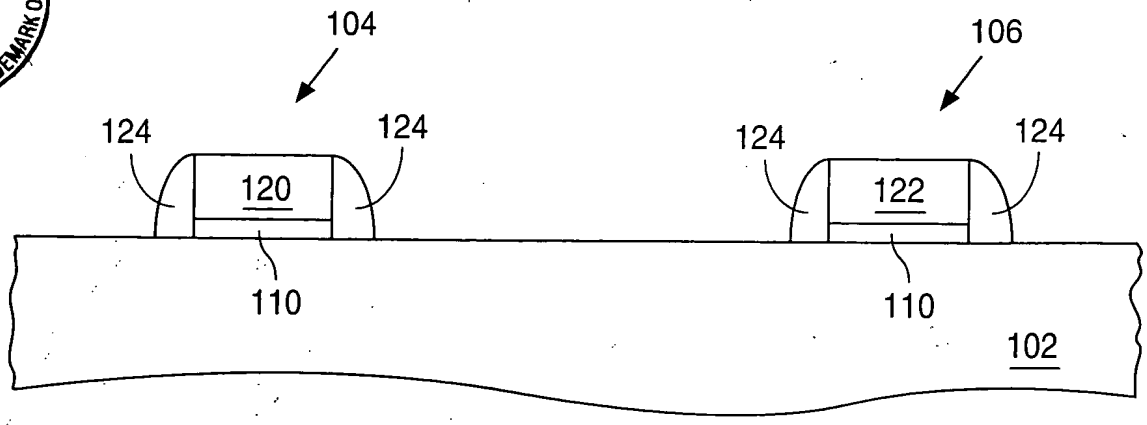

FIG. 4

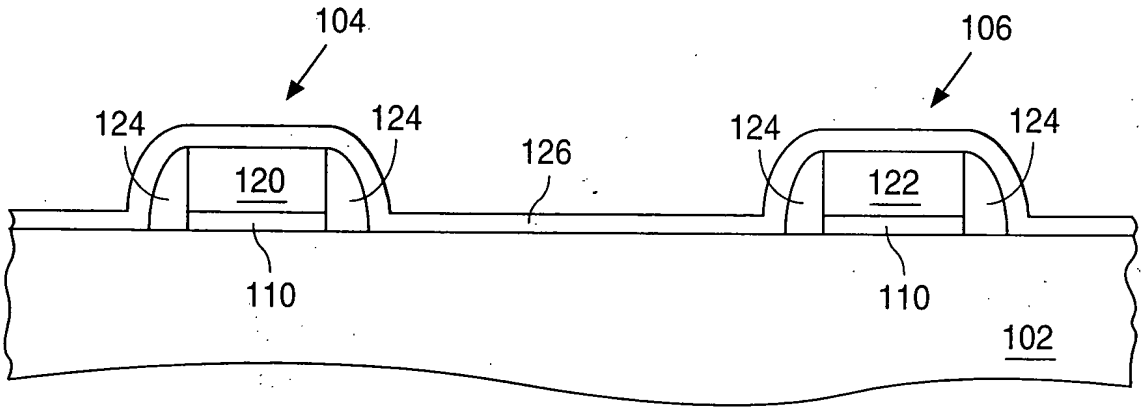

FIG. 5

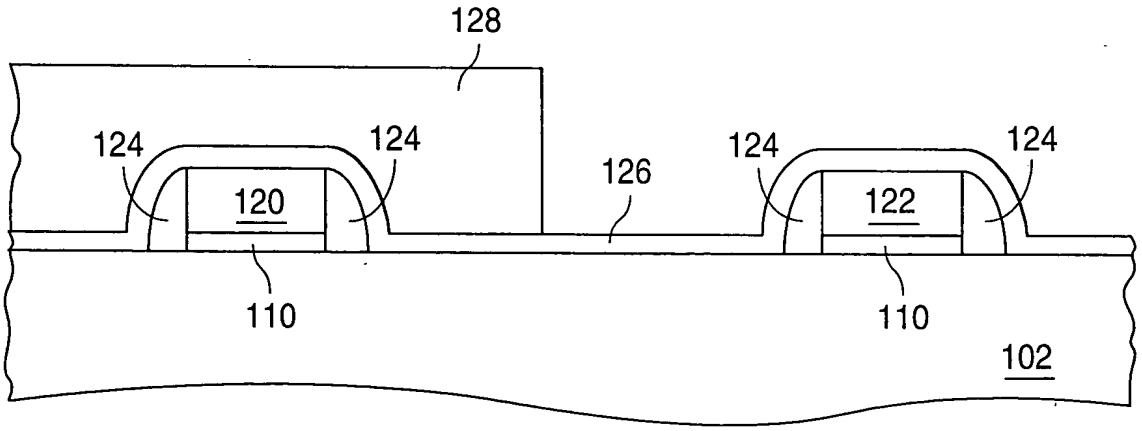

FIG. 6

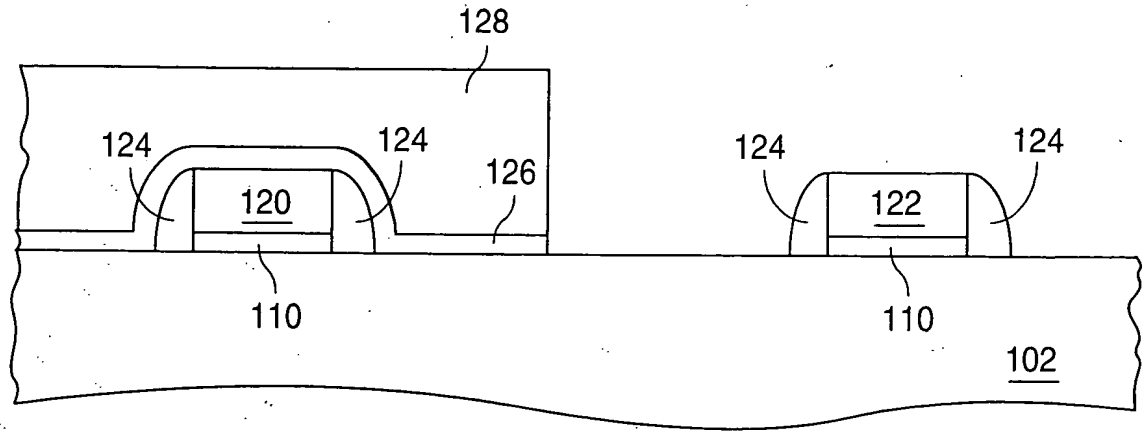

FIG. 7

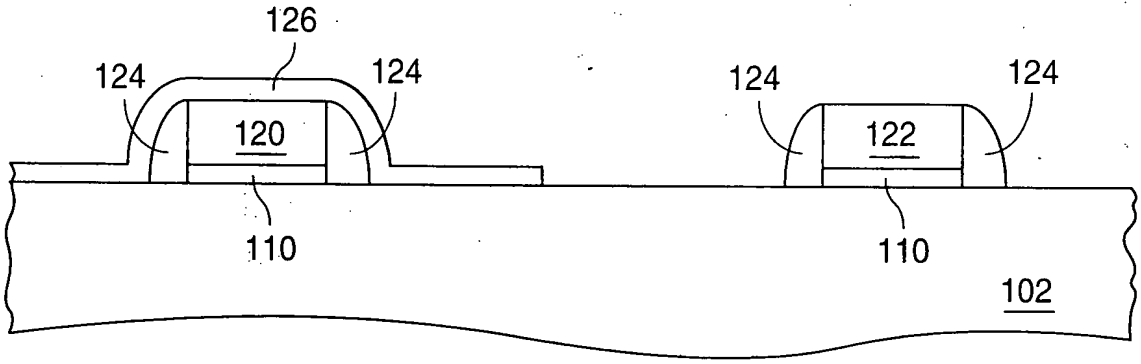

FIG. 8

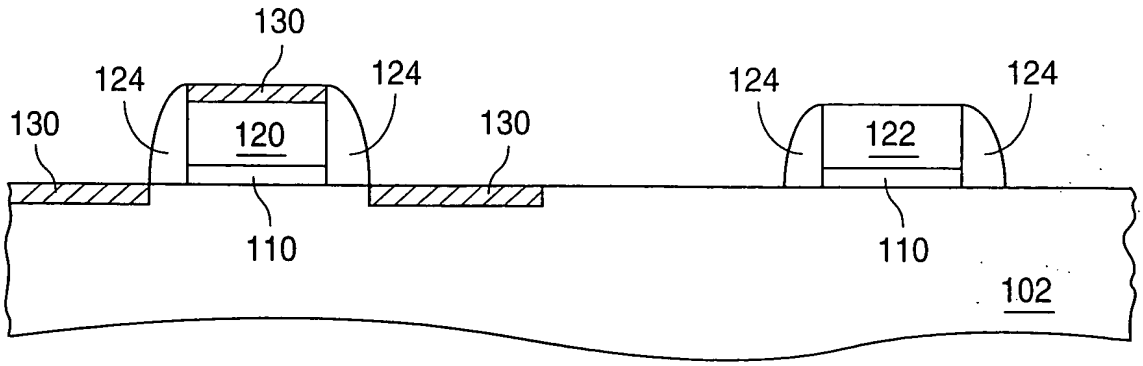

FIG. 9